DATA SHEET

SA56613-XX

5 V, 150 mA LDO and independent delayed $\overline{\text{RESET}}$

Product data
Supersedes data of 2002 Mar 25

2003 Oct 30

Philips
Semiconductors

PHILIPS

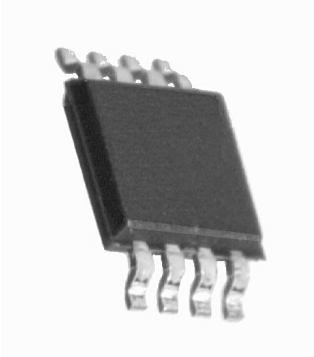
5 V, 150 mA LDO and independent delayed $\overline{\text{RESET}}$ SA56613-XX

DESCRIPTION

The SA56613-XX has a precise fixed 5 V output with a typical accuracy of ±2% to provide very low dropout and low noise in CD-ROM drives, battery-operated systems, and portable computers applications. This regulator consists of an internal voltage reference, an error amplifier, a driver with current limiter and a thermal shutdown.

An Active-LOW $\overline{\text{RESET}}$ is asserted when the regulator output voltage (V_{OUT}) falls below the reset detection voltage threshold. The SA56613-XX is available with fixed detection threshold voltages of 4.2, 4.5, and 4.7 V. The $\overline{\text{RESET}}$ output remains low for 1 ms (typical) when a 10 nF capacitor is connected to C_D pin. The reset time delay can be adjusted by replacing capacitance values from C_D pin to Ground.

The device is available in the small SO8 package (SOP005).



FEATURES

- Very low dropout voltage: 250 mV typ. (I_{out} = 30 mA)
- High precision output voltage: ±2%
- Output current capacity: 150 mA
- Low Noise: 200 μV_{rms} typ. @ 20 Hz to 80 kHz and for I_{OUT} = 30 mA
- Extremely good line regulation: 10 mV typical
- Very good load regulation: 40 mV typical
- Low temperature drift co-efficient to V_{OUT}: ±100 ppm/°C
- Internal current limit and thermal shut-down circuits
- Adjustment-free reset detection voltages: 4.2 V typ., 4.5 V typ. and 4.7 V typ.
- Delay time can be adjusted by external capacitor.
- Wide operating temperature range: –40 °C to +85 °C

APPLICATIONS

- TV and monitors
- Electronic notebooks, PDAs and Palmtop computers
- Cameras, VCRs and camcorders
- PCMCIA cards and CD-ROM drives
- Modems
- Battery-powered or hand-held instruments

SIMPLIFIED SYSTEM DIAGRAM

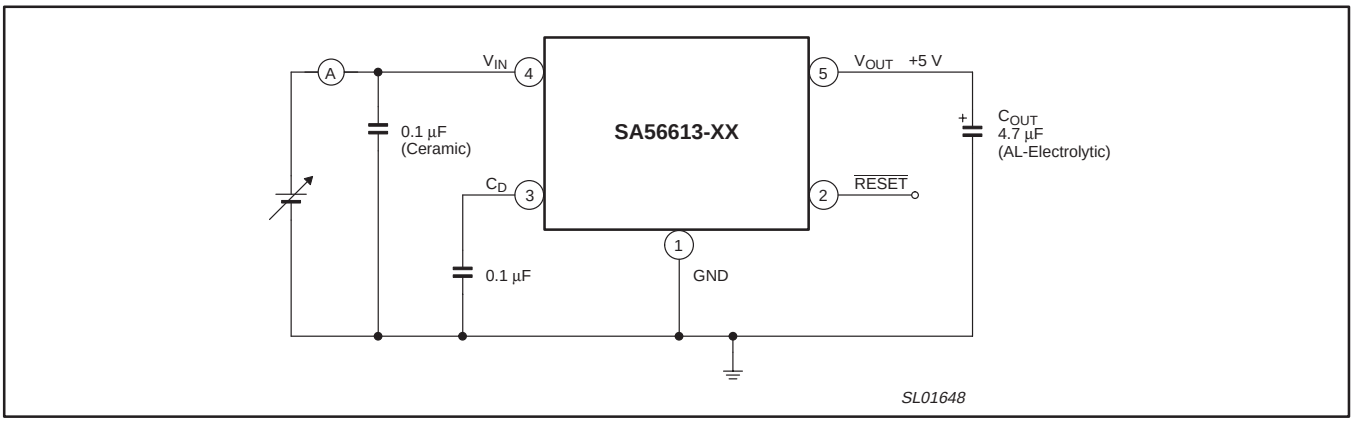


Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
SA56613-**XX**D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOP005	–40 to +85 °C

NOTE:
The device has 3 voltage options, indicated by the XX on the 'Type number'.

XX	OUTPUT VOLTAGE (Typical)	RESET THRESHOLD (Typical)
42	5.0 V	4.2 V
45	5.0 V	4.5 V
47	5.0 V	4.7 V

PIN CONFIGURATION

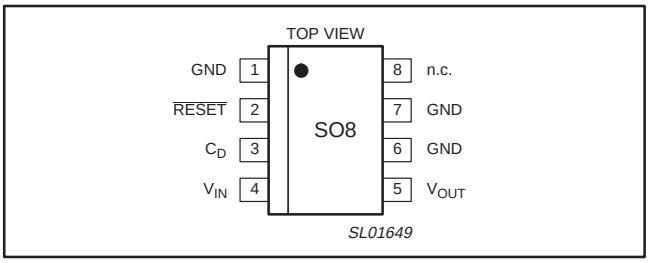


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Ground
2	$\overline{\text{RESET}}$	Active-LOW reset signal output pin. The output remains LOW while V_{OUT} is below V_{SH}, the reset threshold, and for an external set time delay C_D pin after V_{OUT} rises above reset threshold.
3	C_D	Reset delay time capacitor pin. $\overline{\text{RESET}}$ pin output delay time can be set by the capacitance connected to the C_D pin. $t_{PLH} = 10^5 \times C$ where: t_{PLH} = transmission delay time (s) C = capacitor value (F)
4	V_{IN}	Supply voltage input pin
5	V_{OUT}	Regulated output voltage pin
6	GND	Ground pin and heat sink
7	GND	Ground pin and heat sink
8	n.c.	not connected

MAXIMUM RATINGS

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
V_{IN}	Input supply voltage		–0.3	+18	V
I_{OUT}	Output current		–	200	mA
T_{opr}	Operating ambient temperature		–40	+85	°C
T_{stg}	Storage temperature		–40	+150	°C
$T_{j(max)}$	Maximum junction temperature		–	+125	°C
P_D	Power dissipation (Note 1)	Derate 6.5 mW/°C above T_{amb} 25 °C	–	650	mW

NOTE:
1. When mounted on a 55 × 20 mm paper phenol board.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, Figure 13 “Test circuit”, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CCq1}	No-load input current 1	V_{IN} = 6 V; I_{OUT} = 0 mA	–	400	800	μA
I_{CCq2}	No-load input current 2	V_{IN} = 4 V; I_{OUT} = 0 mA	–	2.5	–	μA
Regulator						
V_{OUT}	Output voltage	V_{IN} = 6 V; I_{OUT} = 30 mA	4.90	5.00	5.10	V
$V_{i/o(dif)}$	Input/output differential voltage	V_{IN} = 4.8 V; I_{OUT} = 150 mA	–	0.25	0.5	V
ΔV_1	Line regulation	V_{IN} = 6 V → 10 V; I_{OUT} = 30 mA	–	10	30	mV
ΔV_2	Load regulation	V_{IN} = 6 V; I_{OUT} = 0 mA → 150 mA	–	40	80	mV
$\Delta V_{OUT}/\Delta T$	V_{OUT} temperature coefficient (Note 1)	T_j = –20 °C → +85 °C; V_{IN} = 6 V; I_{OUT} = 30 mA	–	100	–	ppm/°C
RR	Ripple rejection (Note 1)	V_{IN} = 6 V; f = 120 Hz; V_{RIPPLE} = 1 V_{p-p}; I_{OUT} = 30 mA	50	60	–	dB
$V_{n(o)}$	Noise output voltage (Note 1)	V_{IN} = 6 V; f = 20 ~ 80 kHz; I_{OUT} = 30 mA	–	200	400	μV_{rms}
Reset						
V_S	Detection voltage	V_{IN} = H → L				
		SA56613–42	4.03	4.20	4.37	V
		SA56613–45	4.31	4.50	4.69	V
		SA56613–47	4.51	4.70	4.89	V
$\Delta V_S/\Delta T$	V_S temperature coefficient (Note 1)	T_j = –20 °C → +85 °C	–	100	–	ppm/°C
ΔV_S	Hysteresis voltage	V_{IN} = H → L → H	25	50	100	mV
V_{OL}	LOW-level output voltage	V_{IN} = 3.9 V; R_L = 4.7 kΩ	–	100	200	mV
t_{PLH1}	Reset delay time	V_{IN} = 4 V → 5 V; C_D = 0.1 μF	5	10	15	ms
t_{PHL}	‘L’ transmission delay time (Note 1)	V_{IN} = 5 V → 4 V; C_D = 0.1 μF	–	30	90	μs
V_{OPL}	Threshold operating voltage	V_{OL} = 0.4 V	–	0.65	0.85	V

NOTE:
1. This parameter is guaranteed by design.

TYPICAL PERFORMANCE CURVES (SA56613-42D)

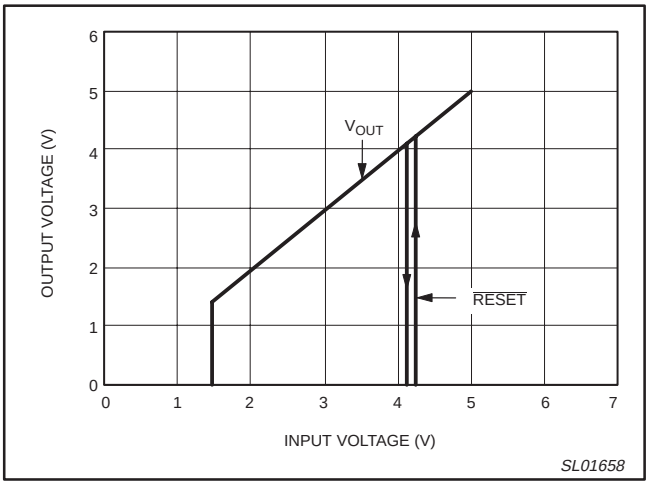


Figure 3. Detection voltage (I_{OUT} = 0 mA).

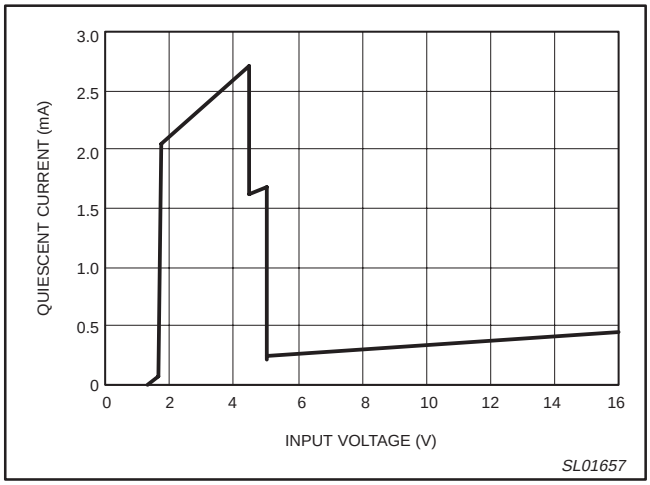


Figure 4. Quiescent current (I_{OUT} = 0 mA).

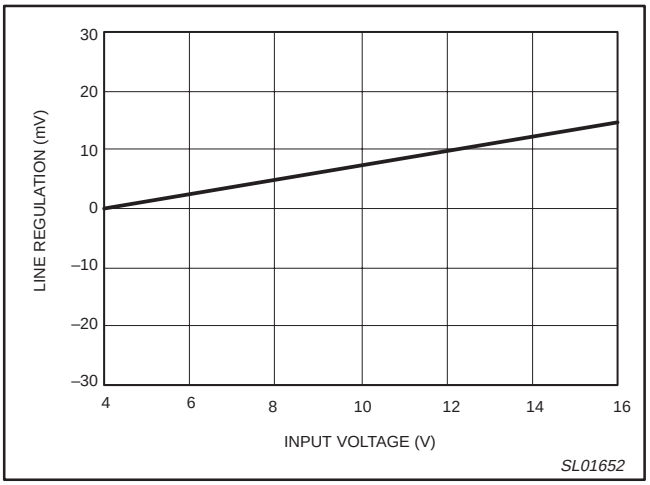


Figure 5. Line regulation.

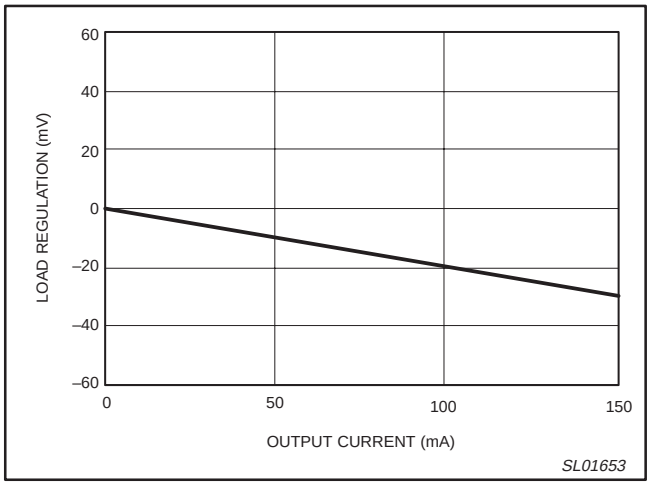


Figure 6. Load regulation.

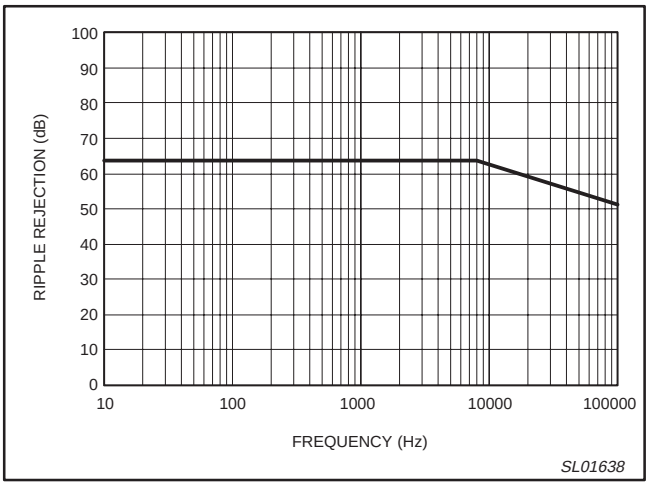


Figure 7. Ripple rejection.

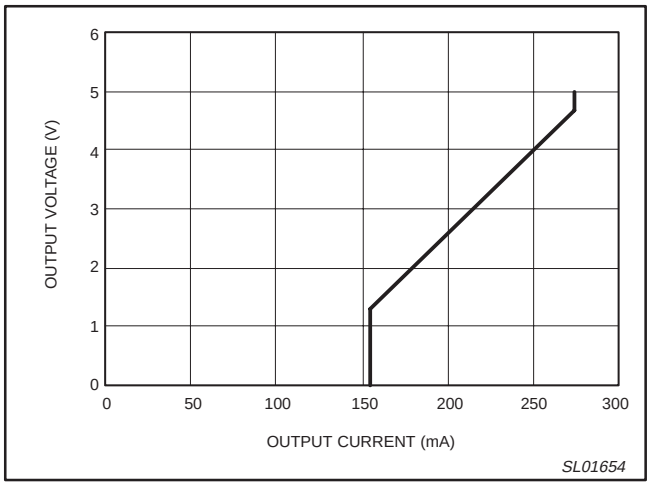


Figure 8. Current limit.

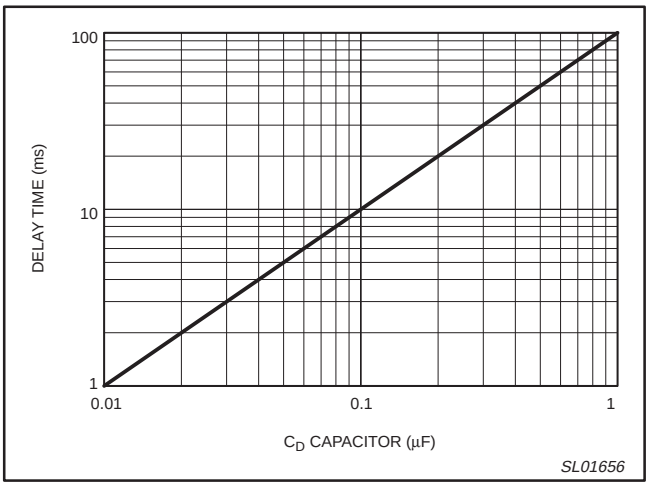


Figure 9. Reset delay time.

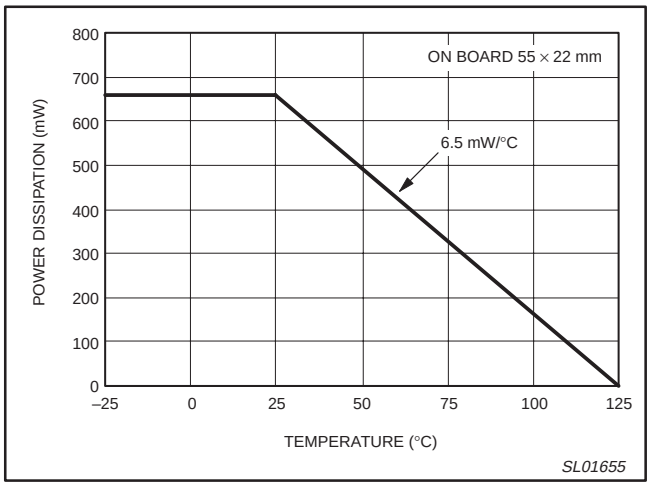


Figure 10. Power dissipation.

TIMING DIAGRAM

The Timing Diagram in Figure 11 depicts the operation of the device. Letters A-I on the Time axis indicates specific events.

A: At "A", V_{OUT} abruptly begins to increase. Also the $\overline{\text{RESET}}$ voltage initially increases but abruptly decreases when V_{OUT} reaches the threshold operating level (typically 0.65 V) that activates the internal bias circuitry and $\overline{\text{RESET}}$ is asserted.

B: At "B",V_{OUT} reaches the threshold level of V_{SH}. At this point the delay time, t_{PLH} is initiated while V_{OUT} rises above V_{SH} to its normal operating level of 5 V. The $\overline{\text{RESET}}$ voltage remains LOW.

C: At "C", V_{OUT} is above V_{SL} and the delay time, t_{PLH} elapses. At this instant, the device releases the hold on the $\overline{\text{RESET}}$. The reset output then goes HIGH. In a microprocessor based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

D-E: At "D", V_{IN} falls below 5 V, causing V_{OUT} to follow. V_{OUT} continues to fall until the V_{SL} undervoltage detection threshold is reached at "E". This causes a reset signal to be generated ($\overline{\text{RESET}}$ goes LOW).

E-F: Between "E" and "F", V_{OUT} continues to fall and then starts rising.

F: At "F", V_{OUT} rises to the V_{SH} level. Once again, the device initiates the delay timer.

F-G: V_{OUT} rises above V_{SH} and returns to normal 5 V output. At "G", the delay (t_{PLH}) times out and once again, then it releases the hold on the $\overline{\text{RESET}}$ and it goes HIGH.

G-H: At "G", V_{OUT} is above the upper threshold and begins to fall, causing $\overline{\text{RESET}}$ to follow it. As long as V_{OUT} remains above the V_{SL}, no reset signal will be generated.

H: At event "H", V_{OUT} falls until the V_{SL} undervoltage detection threshold is reached. At this level, a $\overline{\text{RESET}}$ signal is generated and $\overline{\text{RESET}}$ goes LOW.

I: At event "I", V_{OUT} has decreased until normal internal circuit bias is unable to maintain a $\overline{\text{RESET}}$. As a result, V_{CC} may rise to less than 0.65 V. As V_{CC} decreases further, the V_{OUT} reset also decreases to zero.

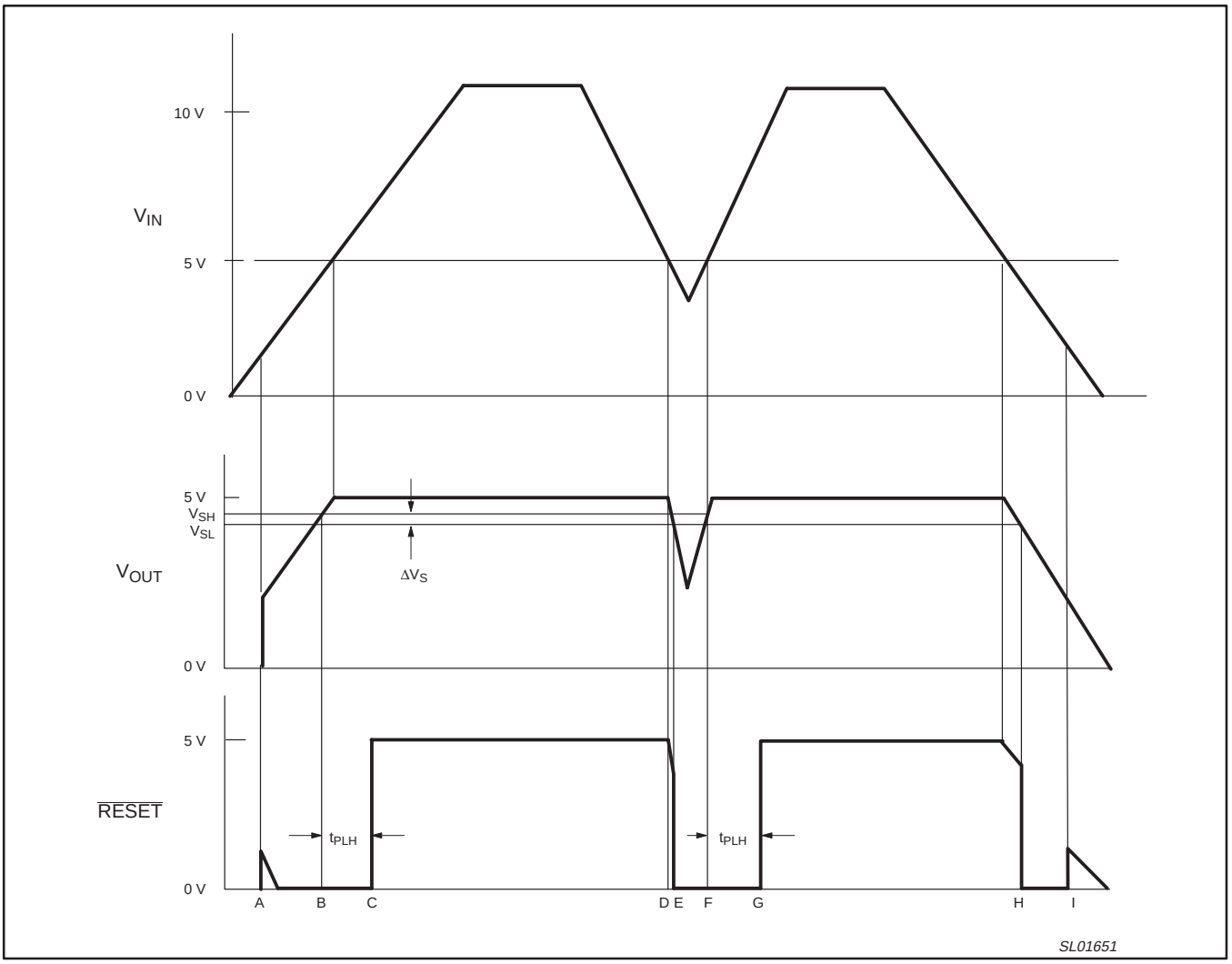


Figure 11. Timing diagram.

APPLICATION INFORMATION

Input capacitor

An input capacitor of ≥1 µF is required to eliminate the AC coupling noise. This capacitor must be located as close as possible to V_{IN} or GND pin (not more than 1 cm) and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitor will work.

Output capacitor

Phase compensation is made for securing stable operation even if the load current varies. For this reason, an output capacitor with good frequency characteristics is needed. Set it as close to the circuit as possible and make the wiring as short as possible.

The value of the output capacitance has to be at least 47 µF connected from V_{OUT} to GND. When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

$\overline{\text{RESET}}$ output

The SA56613-XX has an Active-LOW $\overline{\text{RESET}}$ output. When V_{OUT} of the regulator rises above V_{SH}, the upper detection threshold voltage, the reset delay time is initiated. After the programmed delay time elapses, $\overline{\text{RESET}}$ is released and goes HIGH. The time delay can be set typically from 1 ms to 100 ms by connecting a time delay capacitor from C_D (pin 3) to ground (see Figure 9: $\overline{\text{RESET}}$ Delay time versus C_D, Delay Capacitor).

The $\overline{\text{RESET}}$ delay time (t_{PLH}) can be approximated by the following equation:

$$t_{PLH} = 10^5 \times C \qquad \textbf{Eqn. (1)}$$

(Time is expressed in seconds, Capacitance in Farads.)

For example, for a delay capacitor, C_D of 0.1 µF (100 nF), t_{PLH} is approximately 10 ms.

When the regulator output Voltage falls to or below V_{SL}, the lower detection threshold voltage, the $\overline{\text{RESET}}$ output is asserted and it goes to an Active-LOW state. This “LOW” transmission delay time is typically 30 µs with C_D at 100 nF.

Reset hysteresis voltage

The reset hysteresis voltage, ΔV_S is defined in the following equation:

$$\Delta V_S = V_{SH} - V_{SL} \qquad \textbf{Eqn. (2)}$$

Hysteresis voltage is typically 50 mV. This small level of hysteresis ensures that the reset will not dither when the regulator V_{OUT} is noisy.

PCB layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitors should be kept close to the LDO.

The rise in junction temperature depends on how efficiently the heat is carried away from the junction to ambient. The junction to lead thermal impedance is a characteristic of the package and fixed. The thermal impedance between lead to ambient can be reduced by increasing the copper area on the PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient impedance.

Power dissipation

The SA56613-XX maximum power dissipation depends on the thermal resistance from the die junction to the ambient air. The maximum power dissipation shown in Figure 10 is 650 mW at ambient temperature of 25 °C. It is derated at 6.5 mW/°C above 25 °C.

Power dissipation of the device is $P_D = I_{OUT} (V_{IN} - V_{OUT})$. The maximum power dissipation is:

$$P_{max} = \frac{(T_j - T_{amb})}{(\theta_{JA})} \qquad \textbf{Eqn. (3)}$$

where

$\theta_{JA} = \theta_{JB} + \theta_{BA}$, the junction-to-ambient thermal resistance, θ_{JA} calculated from Figure 10 is 154 °C/W;

θ_{JB} is the thermal resistance from the die junction to PCB material and copper traces;

θ_{BA} is the thermal resistance from the PCB material and copper traces to the surrounding air.

The GND pin provides an electrical connection to ground and a path for heat transfer from the device to the PCB and to the surrounding air. To maximize heat transfer, connect the GND pin to a large ground pad or ground plane.

The following example determines the maximum I_{OUT} at T_{amb} = 25 °C for V_{IN} = 1 V.

$$I_{OUT} = \frac{P_D}{(V_{IN} - V_{OUT})} = \frac{650\ mW}{(12 - 5)} = 92.8mA \qquad \textbf{Eqn. (4)}$$

The maximum output current of the SA56613-XX is reduced as the input voltage, V_{IN} and the ambient temperature, T_{amb} increase.

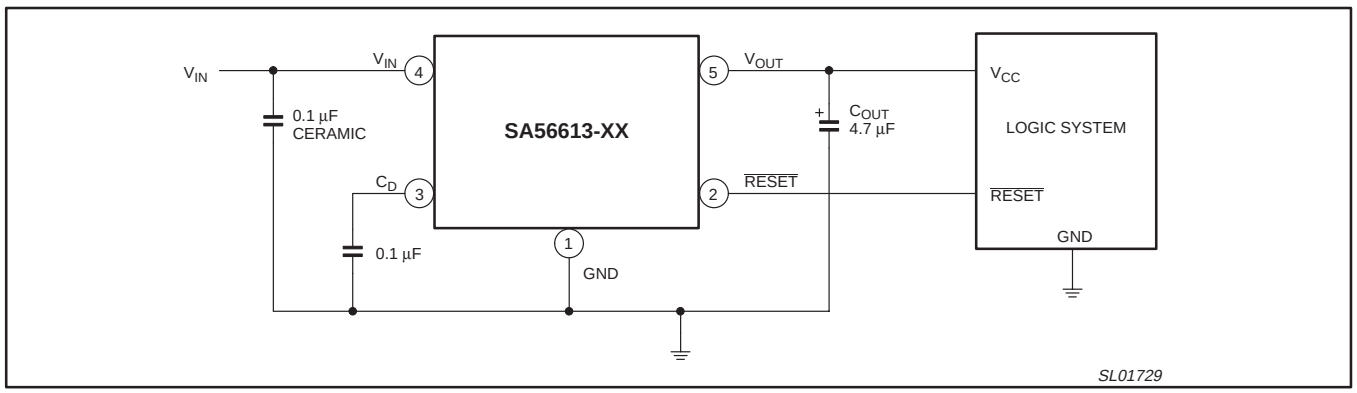


Figure 12. Typical application circuit.

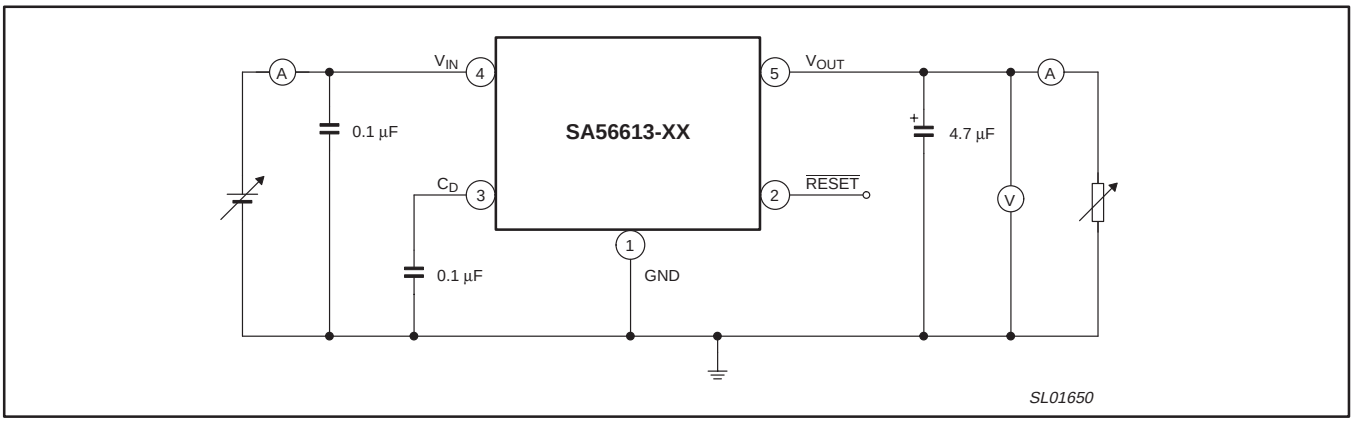


Figure 13. Test circuit.

PACKING METHOD

The SA56613-XX is packed in reels, as shown in Figure 14.

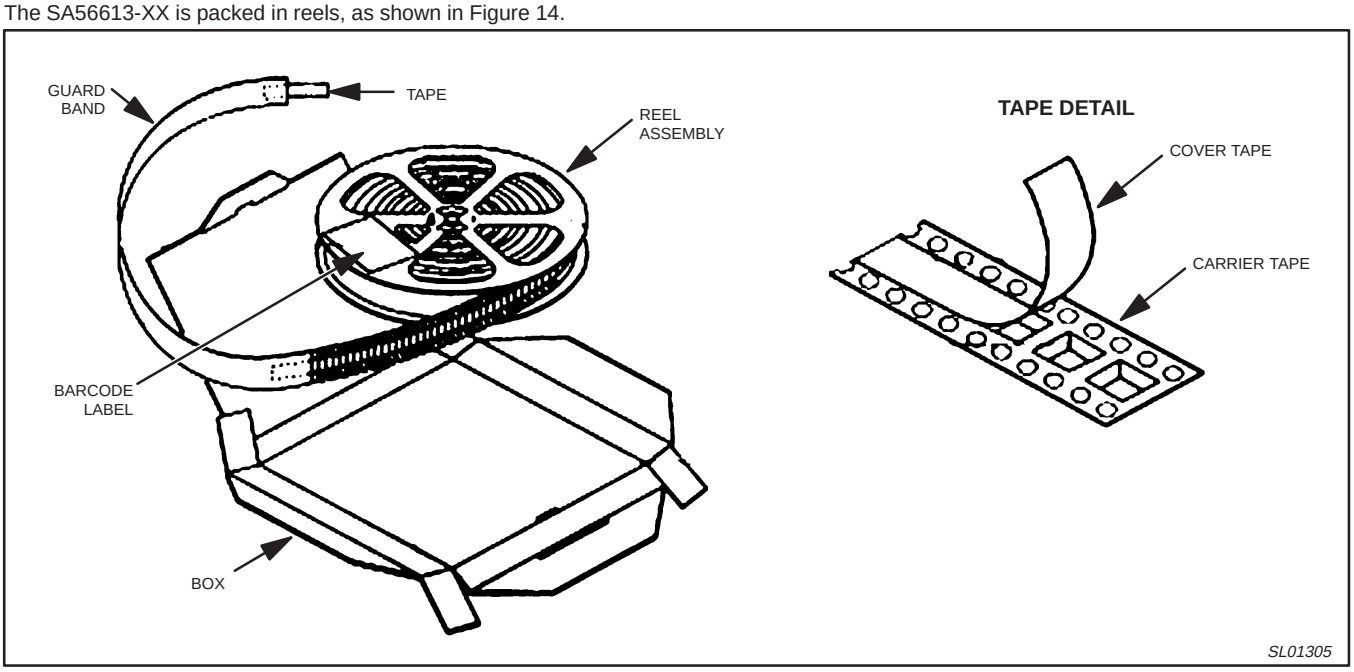
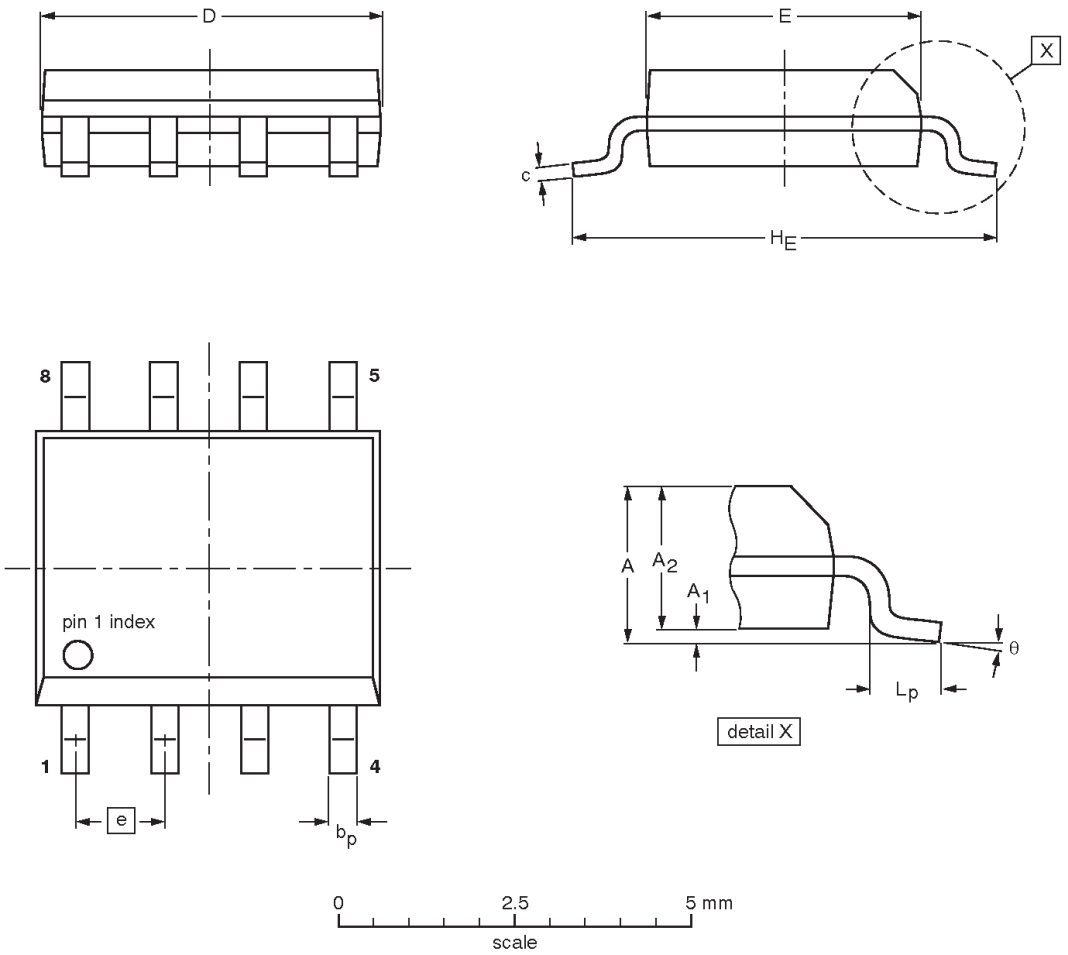


Figure 14. Tape and reel packing method.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOP005**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	b_p	c	D(1)	E(2)	e	H_E	L_p	θ
mm	1.73	0.25 0.10	1.45 1.25	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8	1.27 0.38	8^o 0^o
inches	0.068	0.010 0.004	0.057 0.049	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.050 0.015	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP005	076E03	MS-012				03-10-07

REVISION HISTORY

Rev	Date	Description
_1	20031030	**Product data (9397 750 12214). ECN 853-2331 30323 of 09 September 2003. Supersedes data of 2002 Mar 25 (9397 750 10039).** Modifications: ● Change package outline version to SOP005 in Ordering information table and Package outline sections.
_1	20020325	**Product data (9397 750 10039). ECN 853-2331 27919 of 25 March 2002.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

Date of release: 10-03

Document order number: 9397 750 12214

Let's make things better.

Philips Semiconductors

PHILIPS